What is Claimed is:

1. A memory system comprising:

an address/command bus;

a multidrop data bus having a predetermined number of data signaling lines;

a memory controller to transmit address and command signals on the address/command bus, and to transmit and receive data signals on the multidrop data bus corresponding to the address and command signals; and

first and second memory units, each connected to both the address/command bus and the multidrop data bus, at least the second memory unit comprising controllable termination circuitry having on and off states and coupled to the multidrop data bus, and termination control logic to set the state of the termination circuitry according to decoded commands received on the address/command bus.

2. The memory system of claim 1, wherein the memory controller comprises a command generator capable of generating command signals for a first READ command type when requesting that the first memory unit retrieve data, and command signals for a second READ command type when requesting that the second memory unit retrieve data, the second memory unit having the capability to decode command signals for both the first READ and second READ command types, the second memory unit also having the capability to turn its termination circuitry off in response to receiving a READ command of the second type and turn its termination circuitry on in response to receiving a READ command of the first type.

3. The memory system of claim 2, wherein the first memory unit has termination circuitry, termination control logic, and READ command decode capability similar to that recited for the second memory unit, the first memory unit having the capability to turn its

termination circuitry on in response to receiving a READ command of the second type and turn its termination circuitry off in response to receiving a READ command of the first type.

4. The memory system of claim 1, wherein each memory unit comprises a programmable configuration register capable of storing termination control parameters, the memory controller capable of transmitting termination control parameters to each of the memory units for storage in that unit's configuration register.

5. The memory system of claim 4, capable of supporting a variable number of memory units each having the claimed programmable configuration register, wherein the memory controller is capable of transmitting information dependent on the number of active memory units as part of the termination control parameters.

6. The memory system of claim 1, wherein each memory unit comprises a rank of memory devices, each device in the rank serving a subset of the data bus signaling lines, each memory device having a termination circuit for the data bus signaling lines that it serves, each memory device having termination control logic integrated therein to control that device's termination circuit according to decoded command signals received on the address/command bus.

7. The memory system of claim 6, wherein each memory unit resides on a memory module.

8. The memory system of claim 6, wherein two memory units reside on a memory module.

9. A memory device comprising:

a memory cell array;

a bi-directional data port capable of receiving data for and transmitting data stored in the memory cell array;

an address and command port;

a controllable line termination circuit to terminate signals at the data port, the circuit having on and off states;

an address and command decoder to receive signals at the address and command port; and

termination control logic coupled to the address and command decoder to set the state of the termination circuitry according to decoded commands from the decoder.

10. The memory device of claim 9, the device having a set device ID, wherein the address and command decoder is capable of decoding signals for multiple READ command types, one of which corresponds to the set device ID, the others corresponding to READ commands for other device IDs, the address and command decoder decoding all READ command types but initiating a READ operation only when the received command type corresponds to the set device ID.

11. The memory device of claim 10, wherein the address and command decoder is capable of reporting each READ command type, when received, to the termination control logic, the termination control logic setting the termination circuit state according to the READ command type.

12. The memory device of claim 9, further comprising a register to store parameters for use by the termination control logic.

13. The memory device of claim 12, wherein one of the parameters stored in the register comprises a disable parameter that forces the termination control logic to turn off the line termination circuit.

14. The memory device of claim 12, wherein the termination control logic combines parameters from the register with state signals indicating the state of the memory device and based on decoded commands, to create an enable signal that controls the line termination circuit.

15. A memory controller comprising:

an address/command generator to generate address and command signals for multiple memory units, including READ command signals, wherein the READ command signals identify the memory unit currently being addressed.

16. The memory controller of claim 15, the address/command generator capable of generating address and command signals to transfer termination configuration parameters to memory units connected to the controller.

17. A method of operating a memory device comprising:

terminating an external data bus on the memory device with a controllable line termination circuit having on and off states;

monitoring the state of the memory device; and

setting the state of the line termination circuit based on the state of the memory device.

18. The method of claim 17, further comprising storing line termination parameters, wherein setting the state of the line termination circuit is further based on the state of the parameters.

19. The method of claim 17, further comprising:

decoding read and write commands received from an external memory controller, even when the memory device is not selected for reading or writing by the controller; and

interpreting from the decoded commands the approximate state of the data bus;

wherein setting the state of the line termination circuit is further based on the approximate state of the data bus.

20. The method of claim 19, wherein interpreting the state of the data bus includes determining which of several devices on the data bus is the most current target of a memory read or write transaction, wherein setting the state of the line termination circuit is dependent on which device is the most current target and the type of transaction.

21. The method of claim 20, wherein interpreting the state of the data bus comprises identifying which of several distinguishable read or write commands was received, each of the distinguishable read or write commands corresponding to one of the devices on the data bus.

22. The method of claim 20, further comprising storing line termination parameters

indicative of the number of memory devices sharing the data bus and this memory device's place among those memory devices, and using these parameters along with the determination of which of several devices on the data bus is the current target to set the state of the line termination circuit.

23. The method of claim 22, wherein when this memory device is the only memory device sharing the data bus, the method further comprises disabling the line termination circuit.

24. The method of claim 17, further comprising storing a line termination parameter that, when set, disables the line termination circuit regardless of other state information.

25. A method of operating a memory system having a memory controller and at least two memory units, all connected to a command/address bus and a multidrop data bus, the method comprising:

the memory controller indicating on the command/address bus, when issuing a read or write command to one of the memory units, which memory unit is the target of the command;

each memory unit decoding the issued read or write command; and

each memory unit setting the state of line termination circuitry, having on and off states, based on the decoded command.

26. The method of claim 25, wherein each memory unit also bases setting the state of line termination circuitry on internal parameters unique among the memory units to that unit.

27. The method of claim 26, further comprising the memory controller transmitting at least some of the internal parameters to one of the memory units during an initialization routine, the internal parameters including the number of memory devices present in the system and the position of that memory unit in the system.

28. The method of claim 27, the transmitted parameters including parameters corresponding to the termination state that the memory unit is to enable for specific read and/or write commands.

29. An article of manufacture containing computer instructions that, when executed by a processor, perform a method comprising transferring a register value to a termination parameter register in a memory unit served by a data bus, the register value including fields to indicate, to the memory unit, state conditions under which the memory unit should enable and/or disable a data bus line termination circuit on the memory unit.

30. The article of manufacture of claim 29, the method further comprising evaluating the number of memory units present on the data bus, and selecting the register value for the memory unit according to the number of units present.